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SESSION VIII A: 256K/1Mb DRAMs: I

WPM 8A.3: A Capacitance-Coupled Bit-Line Cell for Mb Level DRAMs

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CIRCUIT TECHNIQUES developed for a stacked capacitor 256Kb NMOS DRAM test model to achieve the best use of a small cell (38.25μm^2) used as a storage element will be reported.

In the development of next generation DRAMs, a certain storage capacitance value (approximately 50fF) must be assembled in the small cell area with minimal capture rate of minority carriers in the substrate. Conventional double polysilicon cells are becoming obsolete for these requirements. Among several improved cell structures, the stacked capacitor cell[1] affords larger storage capacitance by extending the storage region onto the transfer gate. The use of capacitive-coupled bit lines (CCB) in triple polysilicon cell structures are similar, but have an approximately 1.5 times larger storage area, because the total cell area is utilized for the capacitor. Figure 1 shows a plane and cross sectional view of the cell. A large storage area was created by reciprocally connecting the transfer-gate and the capacitor. This has eliminated the space for a contact hole between bit line to cell.

The cell output voltage of CCB and standard metal bit line structures were compared: Figure 2 shows the calculated output voltage as a function of cell size. Lateral dimensions including storage capacitors were assumed to vary with cell size, while the spacing between capacitors and the metal bit line width were kept constant because the minimum line width and the spacing were assumed. Vertical dimensions were also kept constant. A two-dimensional numerical analysis method was used for capacitance evaluation, and the effects of capacitance between adjacent bit lines were taken into account. Since the bit line width of CCB structures varies with cell size, the parasitic capacitance is comparably large for cell sizes over 40μm^2 and the output voltage is lower than that for metal bit line structure. But if the memory cells are very small, the situation is reversed; the capacitance of metal bit lines does not reduce much with cell size due to fringe capacitance components and the emergence of capacitance between bit lines, while the capacitor area rapidly decreases. For the same output voltages, a CCB cell with larger storage capacitance is more resistive to soft errors and superior performance is expected from very small cells.

The cell's operational biases are slightly different from conventional cells. In write operations, bit lines are set at the V_{cc} or V_{ss} level according to the data being written. The voltage source lines provide a V_{cc} level to each storage node via the transfer-gates. Bit lines are then set at the V_{cc} level after closing the transfer-gates, and the storage node of each cell is boosted to near the V_{cc} or $2V_{cc}$ level, respectively. Figure 3 shows the simulated waveforms for a storage node and bit lines of the experimental DRAM.

Figure 4 shows a microscopic photograph of a test chip. Although the design rules resemble those of commercial 256Kb DRAMs, the cell size is one half that of the RAMs or 38.25μm^2. The storage capacitance is 59fF for a polysilicon-to-polysilicon capacitor. Table 1 lists the features of a chip. Relaxed design rules allow for shrinking the cell for 1Mb RAMs. The peripheral circuits were designed with almost the same design rules for the cell, which makes circuit layouts differ from those of ordinary chips, since the cell is too small. Figure 5 shows a circuit inherent to the cell. A sense amplifier is shared by two pair of folded bit lines and is switched by row address A8 to match the cell pitch. Row decoders and drivers are placed on both sides of the cell array, driving one of two word lines alternately to make room for word line pull down latch circuits. A capacitance coupled dummy cell[2] was used for reference voltage generation. The voltage source lines are connected to a V_{cc} metal line at every 64thcell. Simultaneously, polysilicon word lines are shunted by a metal layer to reduce the time constant to 2ns.

Acknowledgments

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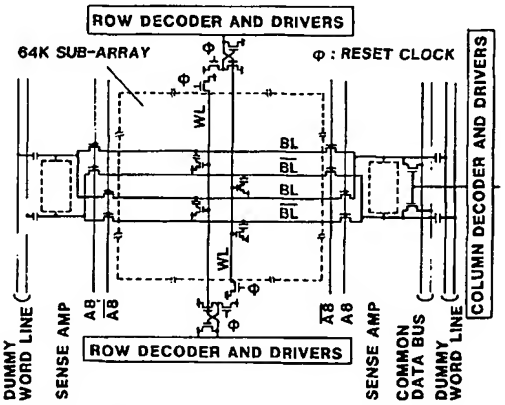

FIGURE 5—Peripheral circuit layout for CCB cells. A sense amplifier block includes precharge and active restore circuits.

[1] Koyanagi, M., Sunami, H. and Hashimoto, N., "Novel High Density, Stacked Capacitor MOS RAM", Proc. 10th Conf. Solid-State Devices, Tokyo 1978, supplement 18-1, p. 35-42; 1979.

[2] Nakano, T., Yabu, T., Noguchi, E., Shirai, K. and Miyasaka, K., "A Sub 100ns 256K DRAM", ISSCC DIGEST OF TECHNICAL PAPERS, p. 224-225; Feb., 1983.

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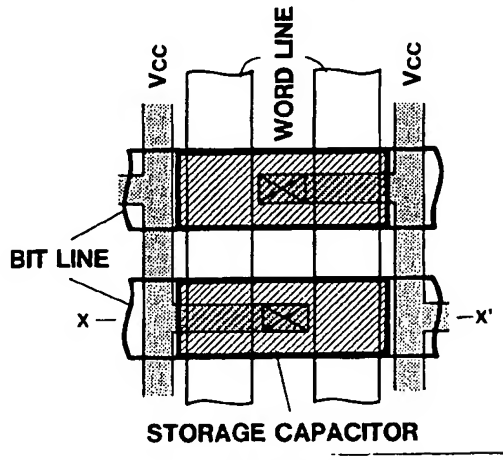


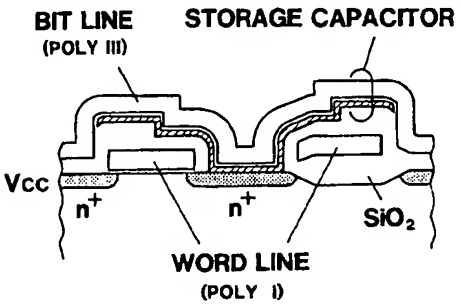
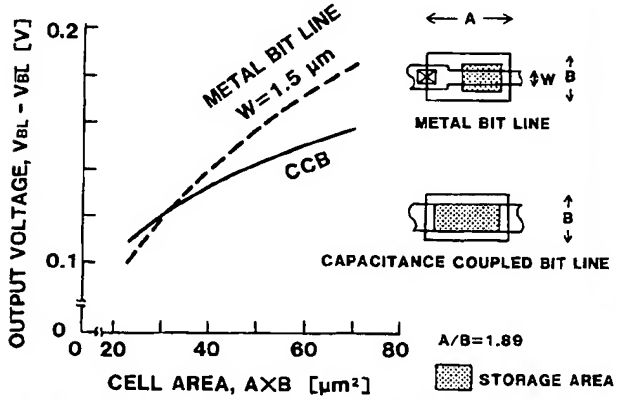


FIGURE 1—(*a-top*)—CCB cell structure, x-x′ cross section; (*b-bottom*)—CCB cell structure, plane view of two cells.

Organization	262144 x 1b
Power supply	5V
Process technology	Triple layer polysilicon Single layer aluminum
Chip size	4.72mm x 7.4mm
Cell size	4.5μm x 8.5μm
Refresh	256 cycles
Transfer-gate length	2.2μm
Peripheral circuit gate length	2.5μm
Minimum line width	1.5μm
Gate oxide thickness	35nm
Capacitor insulator thickness	12nm

TABLE 1—Test device features.



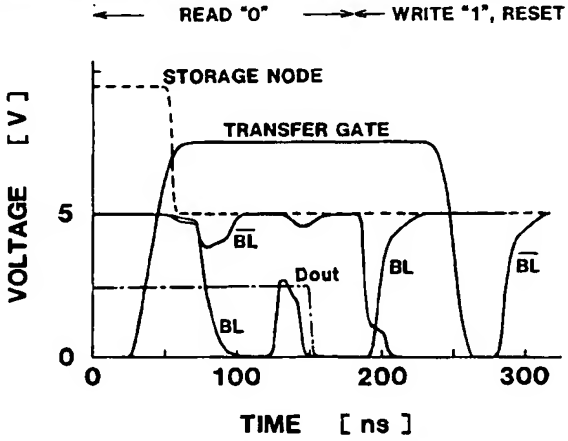
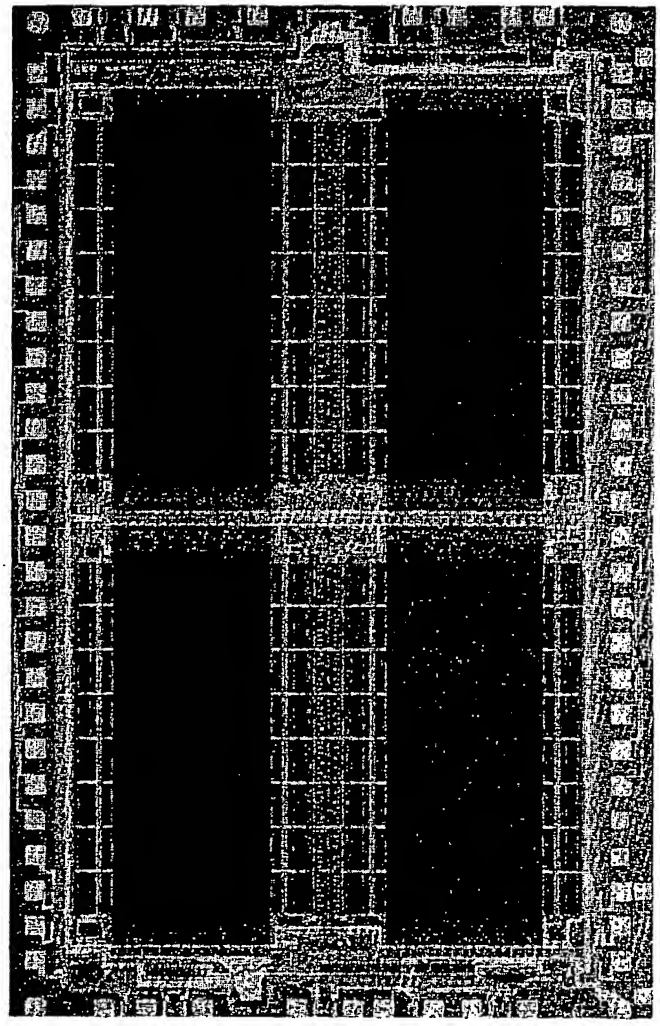


FIGURE 3—Simulated waveforms of CCB cell operations.

[Below]

FIGURE 4—Microphoto of CCB cell 256Kb DRAM chip including monitor transistors and cells.



[Left]

FIGURE 2—Cell output voltage versus cell area: 2.8fF/μm^2 for storage capacitor and 5V for the precharge voltage.